

## **Shallow-Mesa Structure for Planar PIN and APD Photodiodes**

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### Field of the Invention

[0001] This invention relates generally to semiconductor devices, and more specifically to the structure of PIN photodiodes and APDs.

### Cross-Reference To Related Applications

[0002] This application claims priority to United States Provisional Patent Application Serial No. 60/245,902, filed on November 3, 2000.

### Background of the Invention

[0003] For high-bit-rate, long-haul fiber-optic communications p-doped/ intrinsic/ n-doped (PIN) photodiodes and avalanche photodiodes (APDs) are frequently used as photodetectors due to their high sensitivity and bandwidth. Planar and mesa structures are two commonly used configurations for PIN Photodiodes and APDs. Mesa structure PIN photodiodes and APDs are sometimes grown by molecular beam epitaxy (MBE) or metalorganic chemical vapor deposition (MOCVD). These fabrication techniques allow the thickness of the layers and the wafer to be accurately controlled.

[0004] Referring to FIG. 1, a mesa structure PIN 2 known in the prior art is shown. The structure includes a top metal contact 8, two bottoms metal contacts 12, a p-doped Indium Gallium Arsenide (InGaAs) ohmic contact layer 64 lattice matched to Indium

Phosphide (InP), a p-doped InP layer 68, an intrinsic narrow bandgap InGaAs absorption layer 76 lattice matched to InP, a n-doped InP layer 80, and passivation regions 32.

[0005] In fabrication after the layers 80, 76, 68, 64 are sequentially deposited, the mesa structure 84 is formed by chemical etching through the p-doped layers 64, 68 and the intrinsic absorption layer 76. Next, the exposed sidewalls of the p-doped layers 64, 68 and the intrinsic absorption layer 76 that define the mesa structure 84 are passivated with dielectric materials, such as SiO<sub>2</sub> or SiN<sub>x</sub>. As part of this process, defects are inevitably introduced into the p-doped layers 64, 68 and the intrinsic absorption layer 76. The intrinsic InGaAs absorption layer 76 has a low bandgap and the mesa etching introduced defects create extra intraband energy levels. These in turn lead to a high dark current. The dark current in InGaAs PIN photodiodes and APDs fabricated according to the above method is one factor in the generally low reliability of these devices. The low reliability of these devices includes low sensitivity and high noise. These disadvantages significantly restrict the use of InGaAs PIN photodiodes and APDs in optical communications systems.

[0006] Referring to FIG. 2, a planar structure PIN photodiode 4 known in the prior art is shown. The structure 4 includes a top metal contact 8, two bottom metal contacts 12, an intrinsic InGaAs layer 16, an intrinsic InP layer 20, an intrinsic absorption InGaAs layer 76, a n-doped InP layer 28, passivation regions 32, a p-doped InGaAs diffusion region 36, and a p-doped InP diffusion region 40.

[0007] During fabrication of the planar structure PIN photodiode 4, the n-doped InP layer 28, the intrinsic InGaAs layer 76, the intrinsic layer InP 20, and the intrinsic InGaAs layer 16 are sequentially deposited. The p-doped regions 36 and 40 are then formed by diffusing, for example, Zinc (Zn) or Cadmium into the top central region of the device 4. After the diffusion step, the top metal contact 8 and the passivation regions 32 are added.

[0008] Although avoiding the introduction of defects into the intrinsic InGaAs layer 76 during passivation, planar structure PIN photodiodes 4 have disadvantages in device performance and design flexibility. The introduction of the p-dopant by diffusion is not a precise process, and, therefore, the thickness of the p-doped regions 36 and 40 cannot be accurately controlled. In some instances the p-dopant diffuses into the intrinsic InGaAs layer 76. In other instances the p-dopant does not diffuse completely through the intrinsic InP layer 20, or even through the intrinsic InGaAs layer 76. Another disadvantage of planar structure PIN photodiodes 4 is their higher parasitic capacitance. The parasitic capacitance exists between the conductive substrate and device pad. Mesa structure devices can avoid this problem, however, by employing a semi-insulating substrate.

[0009] An additional disadvantage of planar structure PIN photodiodes 4 is that their fabrication process is complex. In particular, the diffusion process requires that the surface of the layer to be doped be carefully prepared. A further disadvantage of planar structure PIN photodiodes 4 is the control of hazardous materials as part of the dopant

diffusion. For example, in Zn diffusion, As, P,  $\text{Zn}_3\text{P}_2$ , and  $\text{Zn}_3\text{As}_2$ , are heated to approximately 550C. At this temperature, small evaporated and inhaled doses are lethal.

**[0010]** What is needed are PIN photodiodes and APDs that overcome the disadvantages of current PIN photodiodes and APDs.

### Summary of the Invention

**[0011]** In one aspect the invention relates to a high bandwidth shallow mesa semiconductor photodiode responsive to incident electromagnetic radiation. The photodiode includes an absorption narrow bandgap layer, a wide bandgap layer disposed substantially adjacent to the absorption layer, a first doped layer having a first conductivity type disposed substantially adjacent to the wide bandgap layer, and a passivation region disposed substantially adjacent to the wide bandgap layer and the first doped layer.

**[0012]** In one embodiment, the photodiode also includes a second doped layer disposed substantially adjacent to the absorption narrow bandgap layer. In another embodiment the photodiode also includes a third doped layer disposed substantially adjacent to the first doped layer and adapted to form an ohmic contact with a substantially adjacent metalization layer. In an additional embodiment, the photodiode also includes a second doped layer and an impact layer disposed substantially adjacent to the second doped layer and the absorption narrow bandgap layer. The ratio of the ionization coefficient for electrons relative to the ionization coefficient for holes for the

impact layer is larger than the corresponding ratio for the absorption narrow bandgap layer, the wide bandgap layer, the first doped layer, and the second doped layer.

[0013] In a further embodiment, the first doped layer includes indium phosphide. In yet another embodiment, the absorption layer comprises indium gallium arsenide. In yet an additional embodiment, the wide bandgap layer varies in thickness from a deposition thickness  $t_1$  to an etching thickness  $t_2$ .

[0014] In another aspect the invention relates a method for fabricating high bandwidth shallow mesa semiconductor photodiode responsive to incident electromagnetic radiation. The method includes generating an absorption narrow bandgap layer, generating a wide bandgap layer disposed substantially adjacent to the absorption narrow bandgap layer, generating a first doped layer disposed substantially adjacent to the wide bandgap layer. The first doped layer has a first conductivity type. The method also includes etching a region of the first doped layer, etching a region of the intrinsic wide bandgap layer, and generating a passivation layer disposed substantially adjacent to the first doped layer and the intrinsic wide bandgap layer.

#### Brief Description of the Drawings

[0015] The above and further advantages of the invention may be better understood by referring to the following description taken in conjunction with the accompanying drawings, in which:

[0016] FIG. 1 is a mesa PIN photodiode as known to the prior art;

[0017] FIG. 2 is a planar PIN photodiode as known to the prior art;

[0018] FIG. 3 is an embodiment of a PIN photodiode according to the invention;

[0019] FIG. 4 is an embodiment of an avalanche photodiode according to the invention;

[0020] FIG. 5 is a flowchart representation of a method for fabricating a shallow-mesa PIN photodiode according to the invention; and

[0021] FIG. 6 is a flowchart representation of a method for fabricating a shallow-mesa APD according to the invention.

### Detailed Description

[0022] Referring to Fig. 3, one embodiment of a shallow mesa planar PIN photodiode 60 according to the invention is shown. The PIN photodiode 60 includes a top metal contact 8, two bottoms metal contacts 12, a p-doped  $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$  ohmic contact layer 64 latticed matched to InP, a p-doped InP layer 68, a wide bandgap intrinsic InP layer 72, an intrinsic narrow bandgap  $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$  absorption layer 76 lattice matched to InP, a n-doped InP layer 80, and passivation regions 32.

[0023] In an alternative embodiment, the wide bandgap intrinsic InP layer 72 is replaced with Indium/ Aluminum/ Arsenide ( $\text{In}_x\text{Al}_{1-x}\text{As}$ ) lattice matched to InP. In one embodiment, the shallow mesa planar PIN photodiode 60 operates according to the principles of back illumination. In this embodiment, the photons in an incident beam

pass through the n-doped InP layer 80 and into the intrinsic  $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$  absorption layer 76. In various other embodiments, the thickness of the layers and the dopant concentrations are selected according to Table 1.

Layer	Thickness	Dopant Concentration
p- $\text{In}_x\text{Ga}_{1-x}\text{As}$ layer 64	50 nm	$1 \times 10^{18} - 5 \times 10^{18} \text{ cm}^{-3}$
p-InP layer 68	0.2 – 0.4 $\mu\text{m}$	$1 \times 10^{18} - 5 \times 10^{18} \text{ cm}^{-3}$
i-InP layer 72	0.2 – 0.4 $\mu\text{m}$	Not Applicable
i- $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ layer 76	1 – 3 $\mu\text{m}$	Not Applicable
n-InP layer 80	0.5-1 $\mu\text{m}$	$1 \times 10^{18} - 5 \times 10^{18} \text{ cm}^{-3}$
Table 1		

[0024] As part of fabrication the p-doped  $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$  layer 64, the p-doped InP layer 68, the intrinsic InP layer 72, the intrinsic  $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$  layer 76, and the n-doped InP layer 80 are deposited by MBE or MOCVD techniques. This means that the thickness of the layers 64, 68, 72, 76, 80 can be accurately controlled. Once all the layers 64, 68, 72, 76, 80 have been deposited, the mesa 84' is formed by etching through the p-doped  $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$  layer 64 and the p-doped InP layer 68, and into the intrinsic InP layer 72. The etching process is controlled so that after completion the intrinsic InP layer 72 has a thickness  $t_1$  in the range of 0.1-0.3 $\mu\text{m}$ . The lower bound on this range ensures that the intrinsic  $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$  layer 76 is adequately protected from the introduction of defects from the passivation process. The deposition thickness  $t_2$  of the intrinsic InP layer 72 is chosen so as to minimize the carrier-transit time increase introduced by the additional layer 72.

[0025] In general the introduction of defects into the intrinsic InP layer 72 during the passivation process does not lead to significant surface leakage current. This is due in

part to the wideband gap of InP. In addition, potential dark current from this layer 72 is minimized by closely monitoring the etching process so that little of the sidewall of the intrinsic InP layer 72 is exposed. The passivated region of the InP layer 72 away from the mesa does not produce significant dark current because the electric field is relatively weak in this region. Similarly, the dark current from the p-doped  $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$  layer 64 and the p-doped InP layer 68 is not significant because the electric field in these regions is low.

**[0026]** Due to the confined lateral extent  $W$  of the mesa 84', the electric field 92 is confined below and within the mesa 84'. This design feature defines the photosensitive region of the intrinsic  $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$  layer 76, that is, the area of the intrinsic  $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$  layer 76 containing the electric field 92.

**[0027]** Referring to FIG. 4, one embodiment of a shallow mesa planar APD 120 according to the invention is shown. The structure and fabrication of the upper portion of the APD 120 is similar to the shallow mesa planar PIN photodiode 60 discussed for FIG. 3. In particular, the upper portion includes a top metal contact 8, post-etching passivation regions 32, a p-doped  $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$  layer 64, a p-doped InP layer 68, an intrinsic InP layer 72, and an intrinsic  $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$  absorption layer 76.

**[0028]** The lower portion of the APD photodiode 120 includes an intrinsic InAlGaAs layer 124, a p-doped InAlAs layer 128, an intrinsic InAlAs layer 132 latticed matched to InP, a n-doped InP layer 80, and two bottom metal contacts 12. The intrinsic InAlGaAs layer 124 is present for bandgap matching purposes. The p-doped InAlAs layer 128 is



present to assist in the modulation of the electric field. The intrinsic InAlAs layer 132 provides a region of large electric field to drive the electron impact ionization avalanche process. This is achieved in the APD 120 because the ratio of the ionization coefficient for electrons relative to the ionization coefficient for holes for the intrinsic InAlAs layer 132 is large with respect to the ratios of the other layers 64, 68, 72, 76, 124, 128, 80.

[0029] In alternative embodiments of the shallow mesa planar APD 120, the thickness of the layers 64, 68, 72, 76 is varied as described above in Table 1. In an alternative embodiment, the wide bandgap intrinsic InP layer 72 is replaced with Indium/ Aluminum/ Arsenide ( $\text{In}_x\text{Al}_{1-x}\text{As}$ ) lattice matched to InP. In one embodiment, the shallow mesa planar APD 120 operates according to the principles of back illumination. In this embodiment, the photons in an incident optical beam pass through the n-doped InP layer 80 and into the intrinsic  $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$  absorption layer 76. In various embodiments, the thickness of the layers 124, 128, 80 and their dopant concentrations are selected according to Table 2.

Layer	Thickness	Dopant Concentration
i-InAlGaAs layer 124	0.25 $\mu\text{m}$	Not Applicable
InAlAs layer 128	0.2 – 0.5 $\mu\text{m}$	$1 \times 10^{18} - 5 \times 10^{18} \text{cm}^{-3}$
i- InAlAs layer 132	0.2 – 0.5 $\mu\text{m}$	Not Applicable
n-InP layer 80	0.5-1 $\mu\text{m}$	$1 \times 10^{18} - 5 \times 10^{18} \text{cm}^{-3}$
Table 2		

[0030] Referring to FIG. 5 a flowchart representation of a method 145 for fabricating a shallow-mesa PIN photodiode according to the invention is shown. The method 145 includes generating an absorption narrow bandgap layer (step 150), for example in one

embodiment intrinsic  $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ , and generating a wide bandgap layer (step 155), for example in one embodiment intrinsic InP, substantially adjacent to the narrow bandgap layer. The method 145 also includes generating a first doped layer (step 160), for example in one embodiment p-doped InP, substantially adjacent to the wide bandgap layer. The first doped layer has a first conductivity type. The thickness of the first doped layer is determined in part according to the etching accuracy and is generally small compared to the other layers in order to minimize the carrier transit time increase introduced by its presence. The method 145 additionally includes etching a region of the first doped layer (step 165) and etching a region of the intrinsic wide bandgap layer (step 170). The method 145 further includes generating a passivation region (step 175) disposed substantially adjacent to the first doped layer and the intrinsic wide bandgap layer. In etching the intrinsic wide bandgap layer, the processes of step 170 are designed to ensure that an adequate thickness of the first doped layer remains to protect the absorption narrow bandgap layer from defects introduced during the passivation step 175.

**[0031]** In one embodiment, the method 145 also includes generating a second doped layer (step 180) disposed substantially adjacent to the absorption narrow bandgap layer. In another embodiment, the method 145 also includes generating a third doped layer (step 185) disposed substantially adjacent to the first doped layer and adapted to form an ohmic contact with a substantially adjacent metalization layer.

**[0032]** Referring to FIG. 6 a flowchart representation of a method 190 for fabricating a shallow-mesa APD according to the invention is shown. The operation of the steps

150 through 175 is as described above with respect to FIG. 5. The method shown in FIG. 6 also includes generating a second doped layer (step 195) and generating an impact layer (step 200) disposed substantially adjacent to the second doped layer and the absorption narrow bandgap layer. The impact layer is chosen so that the ratio of the ionization coefficient for electrons relative to the ionization coefficient for holes for the impact layer is larger than the corresponding ratio for the absorption narrow bandgap layer, the wide bandgap layer, the first doped layer, and the second doped layer. In one embodiment, the method 190 also includes generating a third doped layer (step 205) disposed substantially adjacent to the first doped layer and adapted to form an ohmic contact with a substantially adjacent metalization layer.

**[0033]** Those skilled in the art will recognize that the PIN and APD structures in FIGS. 3 and 4, respectively, each represent only a single PIN and APD embodiment and that the principles of the invention can equally well be applied to alternative PIN and APD structures known in the art.

**[0034]** Having described and shown the preferred embodiments of the invention, it will now become apparent to one of skill in the art that other embodiments incorporating the concepts may be used and that many variations are possible which will still be within the scope and spirit of the claimed invention. These embodiments should not be limited to disclosed embodiments but rather should be limited only by the spirit and scope of the following claims.